REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1, 3-5 and 9-39 are pending in the application. The Examiner additionally stated that claims 1, 3-5 and 9-39 are rejected. By this amendment, claims 1, 3, 4, 10, 24, 26, 32, 38, and 39 have been amended. Hence, claims 1, 3-5 and 9-39 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Claims

Rejections Under 35 U.S.C. §102(b)

The Examiner rejected claims 1, 3-5, 9-12, 16-18, 20, 23-25, and 32-39 under 35 U.S.C. 102(b) as being anticipated by Lynch, U.S. Patent 5,930,820 (hereinafter, *Lynch*). Applicant respectfully traverses the Examiner's rejections.

Claim 1

Applicant has amended claim 1 to clarify that the plurality of storage elements store data exclusively specified by push instructions. In contrast, the data cache 34 of *Lynch* does not store data exclusively specified by push instructions; rather, the data cache 34 stores both stack data (in a stack storage 54) and non-stack data (in a conventional cache storage 50). See col. 6, lines 6-7; col. 11, lines 16-26; col. 4, lines 32-35; col. 11, lines 35-39. Furthermore, although the stack storage 54 of *Lynch* stores stack data, Applicant can find no teaching in *Lynch* that his stack storage 54 provides requested data in a first number of clock cycles for pop instructions and provides requested data in a second different number of clock cycles for load instructions.

Claim 3

Claims 3 is directed to a cache memory; whereas the main memory 16 of *Lynch* is not a cache memory, as may be seen from the block diagram of Fig. 1 showing a well-known computer system 10 including a microprocessor 12, bus bridge 14, I/O devices 18, and

main memory 16. Rather, *Lynch* teaches an instruction cache 32 and a data cache 34 within the microprocessor 10, neither of which comprises the main memory 16.

Claim 10

Applicant has amended claim 10 to clarify that the plurality of storage elements store data exclusively specified by push instructions. In contrast, the data cache 34 of *Lynch* does not store data exclusively specified by push instructions; rather, the data cache 34 stores both stack data (in a stack storage 54) and non-stack data (in a conventional cache storage 50). See col. 6, lines 6-7; col. 11, lines 16-26; col. 4, lines 32-35; col. 11, lines 35-39. Furthermore, although the stack storage 54 of *Lynch* stores stack data, Applicant can find no teaching in *Lynch* that his stack storage 54 provides source data from a first subset of the storage elements in a first number of clock cycles if a memory address hits in the first subset, but provides the source data from a second subset of the storage elements in a second different number of clock cycles if the memory address does not hit in the first subset but hits in the second subset.

Claim 16

Claims 16 is directed to a cache memory; whereas the main memory 16 of *Lynch* is not a cache memory, as may be seen from the block diagram of Fig. 1 showing a well-known computer system 10 including a microprocessor 12, bus bridge 14, I/O devices 18, and main memory 16. Rather, *Lynch* teaches an instruction cache 32 and a data cache 34 within the microprocessor 10, neither of which comprise the main memory 16.

Claim 32

Applicant has amended claim 32 to include the step of storing data into a LIFO cache memory exclusively specified by push instructions. The data cache 34 of *Lynch* does not store data exclusively specified by push instructions; rather, the data cache 34 stores both stack data (in a stack storage 54) and non-stack data (in a conventional cache storage 50). See col. 6, lines 6-7; col. 11, lines 16-26; col. 4, lines 32-35; col. 11, lines 35-39. Furthermore, although the stack storage 54 of *Lynch* stores stack data, Applicant can find no teaching in *Lynch* of his stack storage 54 providing requested data in a first number of clock cycles if the request is in response to a pop instruction and providing the requested

data in a second different number of clock cycles if the request is in response to a load instruction.

Claims 38 and 39

Applicant has amended claims 38 and 39 similarly to claims 1 and 10, respectively. For reasons similar to those stated above with respect to claims 1 and 10, respectively, Applicant respectfully requests that the Examiner withdraw his rejection of claims 38 and 39.

The Examiner rejected claim 26 under 35 U.S.C. 102(b) as being anticipated by Matthews, U.S. Patent 5,956,752 (hereinafter, *Matthews*). Applicant respectfully traverses the Examiner's rejections.

Claim 26

Applicant has amended claim 26 to include the step of storing stack data into a cache memory exclusively specified by push instructions. Applicant can find no teaching in *Matthews* of storing stack data into a cache memory exclusively specified by push instructions. In particular, the memory array 160 of *Matthews* does not store data exclusively specified by push instructions.

Rejections Under 35 U.S.C. §103(a)

The Examiner rejected claims 13-15 and 19 under 35 U.S.C. 103(a) as being unpatentable over *Lynch* in view of *Matthews*. Applicant respectfully traverses the Examiner's rejections.

The Examiner rejected claims 27-31 under 35 U.S.C. 103(a) as being unpatentable over *Matthews* in view of *Lynch*. Applicant respectfully traverses the Examiner's rejections.

The Examiner rejected claim 21 under 35 U.S.C. 103(a) as being unpatentable over *Lynch* in view of Healy, U.S. Patent No. 3,810,117 (hereinafter, *Healy*). Applicant respectfully traverses the Examiner's rejections.

The Examiner rejected claim 21 under 35 U.S.C. 103(a) as being unpatentable over *Lynch* in view of Tremblay, U.S. Patent No. 6,038,643 (hereinafter, *Tremblay*). Applicant respectfully traverses the Examiner's rejections.

Claims 3-5 and 9 depend from and add further limitations to claim 1, which is not anticipated by *Lynch* as discussed above. Claims 11-25 depend from and add further limitations to claim 10, which is not anticipated by *Lynch* as discussed above. Claims 27-31 depend from and add further limitations to claim 26, which is not anticipated by *Matthews* as discussed above. Claims 33-39 depend from and add further limitations to claim 32, which is not anticipated by *Lynch* as discussed above.

For these reasons, Applicant respectfully requests that the Examiner withdraw his rejection of claims 1, 3-5 and 9-39.

CONCLUSIONS

In view of the arguments advance above, Applicant respectfully submits that claims 1, 3-5 and 9-39 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

Respectfully submitted,

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Date: _____